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# CONFIGURATION AND METHOD FOR MAKING CONTACT WITH THE BACK SURFACE OF A SEMICONDUCTOR SUBSTRATE

## Cross-Reference to Related Application:

This application is a continuation of copending International Application No. PCT/DE02/00670, filed February 22, 2002, which designated the United States and was not published in English.

## Background of the Invention:

### Field of the Invention:

The present invention relates to a configuration and a method for making contact with the back surface of a semiconductor substrate.

The fabrication of semiconductor components makes use of method steps that require electrical contact to be made with the substrate that is to be processed. This is the case, for example, in electrical or electrochemical process steps. In order to enable a very large number of identical components to be fabricated in parallel on a semiconductor substrate, it is necessary for the substrate to be processed uniformly by the process step. This requires contact-making methods which make electrical contact which is as homogeneous as possible with respect to the substrate. If homogeneous electrical contact

is not ensured, there is a variation in the electrical potential over the substrate, which can make its presence felt by an inhomogeneous process control and prevents uniform execution of the process step. The fluctuation leads to a non-uniform electrodeposition in the case of a negative substrate potential and to a non-uniform anodic dissolution in the case of a positive substrate potential.

In the case of anodic dissolution of the substrate, for example given suitably selected doping and electrolyte composition, pores are formed when there is a low anodic potential and electropolished surfaces are formed when there is a high anodic potential. Therefore, the semiconductor components formed are highly dependent on the applied potential, which can prevent the formation of functioning semiconductor components.

The formation of pores in silicon is of interest, for example, for the manufacture of trench capacitors, since the formation of pores allows the surface area to be increased considerably, with an associated increase in capacitance. What are known as mesopores with a pore diameter in the range from 2 to 10 nanometers (nm) are particularly suitable pores. Since, as has already been mentioned above, the formation of pores is dependent on the electrical potential, it is of considerable importance for this potential to be applied to the substrate

in such a manner that it is distributed as uniformly as possible over the substrate.

By way of example, International Patent Disclosure WO 92/02948 A1, corresponding to U.S. Patent No. 5,324,410, discloses making contact with the wafer back surface with the aid of one or more spring contacts. This too has the drawback that the desired potentials can in each case only be generated locally, and on the wafer back surface the potential may fluctuate at relatively great distances from the contact points. Moreover, a particular drawback is that metal is brought into contact with the wafer. When fabricating integrated circuits with ever smaller feature sizes, a metal contact with the wafer should be ruled out at least in the front end process, for reasons, for example, of particle contamination from particles which become detached.

A known method for producing uniform back-surface contact with a semiconductor substrate over the entire surface is known, for example, in U.S. Patent No. 5,209,833. In this case, electrolyte contact is made with the substrate back surface, ensuring that there is very little fluctuation in the contact resistance between substrate and electrolyte.

However, the method for forming an electrolyte back-surface contact over the entire surface is complex in terms of process technology.

Summary of the Invention:

It is accordingly an object of the invention to provide a configuration and a method for making contact with the back surface of a semiconductor substrate that overcome the above-mentioned disadvantages of the prior art devices and methods of this general type.

With the foregoing and other objects in view there is provided, in accordance with the invention, a configuration for making contact with a semiconductor substrate. The configuration contains a first sealing ring, a second sealing ring being larger than the first sealing ring, and a base body having a base-body surface. The first sealing ring and the second sealing ring are disposed on the base-body surface. The first sealing ring is disposed completely inside a region of the base-body surface surrounded by the second sealing ring. The base body has a first opening and a second opening each starting from the base-body surface and extending between the first sealing ring and the second sealing ring. A semiconductor substrate is provided and has a first main surface and a second main surface. The semiconductor

substrate is disposed on the first sealing ring and the second sealing ring with the first main surface facing the base body. A conductive layer having a surface is disposed on the semiconductor substrate. The conductive layer is disposed such that a current impressed into the conductive layer is uniformly distributed across the first main surface of the semiconductor substrate. A first line system is connected to the first opening for admitting and discharging at least one electrically conductive liquid. A second line system is connected to the second opening for admitting and discharging the electrically conductive liquid. A contact wire is disposed uncovered on the base-body surface of the base body between the first sealing ring and the second sealing ring.

The configuration according to the invention allows homogeneous electrical back-surface contact to be made with the wafer by partial electrolytic contact-making. It contains two sealing rings in a base body. The substrate may, for example, be applied to the sealing rings, and the substrate back surface can be etched clear of an insulator in the circular ring between the two sealing rings, with the result that, for example, a conductive layer which has been applied to the back surface of the substrate is uncovered. Then, an electrolyte can be used to make contact with the uncovered conductive layer between the two sealing rings. The contact used for the electrolyte is the contact wire that is disposed

in the annular strip between the first and second sealing rings. The conductive layer in the substrate makes it possible for the current which has been introduced via the electrolyte contact to be distributed uniformly over the substrate back surface and to flow from the substrate back surface to the substrate front surface.

There is provision for the substrate, which contains a first main surface and a second main surface, to be disposed on the first sealing ring and the second sealing ring.

Furthermore, there is provision for a conductive layer, which has a surface, to be disposed on the first main surface. The conductive layer is used to distribute a current uniformly over the substrate back surface.

Furthermore, there is provision for a first insulating layer, which is removed in the region between the first sealing ring and the second sealing ring, to be disposed on the conductive layer. The removal of the insulating layer between the first and second sealing ring has the advantage that it is possible to form electrical contact with the conductive layer and therefore with the substrate back surface between the first sealing ring and the second sealing ring.

A further advantageous configuration of the invention provides for a cavity to be delimited by the first sealing ring, the second sealing ring, the base body and the substrate. The cavity has the advantage that, for example, an etching substance can be introduced into the cavity, by which the insulating layer can be removed from the conductive layer. Furthermore, the cavity has the advantage that an electrolyte can be introduced into the cavity and can be used to form electrical contact between the contact wire and the conductive layer.

In this case, it is advantageous for that region of the substrate surface which is enclosed between the first sealing ring and the second sealing ring to be formed in the shape of a ring at the wafer edge, since at that location the thickness of an insulating layer is usually lower than in the center of the back surface of the wafer. The insulator layer, which is thinner at the edge, has the advantage that it can be removed more quickly from the conductive layer in the edge region. Furthermore, the etching time required to uncover the conductive layer can be shortened by using special holding clamps during nitride or polysilicon deposition, these clamps reducing deposition in the region between the first sealing ring and the second sealing ring.

With regard to the method, the object is achieved by a method for making contact with a semiconductor substrate. The method includes the steps of:

a) providing a base body, which has a base-body surface, on which a first sealing ring and a second sealing ring are disposed, the first sealing ring being smaller than the second sealing ring and the first sealing ring being disposed completely inside that region of the base-body surface which is surrounded by the second sealing ring;

b) a first opening and a second opening being disposed in the base body, starting from the base-body surface, between the first sealing ring and the second sealing ring;

c) a contact wire being disposed uncovered on the base-body surface of the base body between the first sealing ring and the second sealing ring;

d) providing a substrate which contains a first main surface and a second main surface, a conductive layer being disposed on the first main surface;

e) disposing the first substrate with the first main surface on the first sealing ring and the second sealing ring, a cavity being formed, which is delimited by the first sealing

ring, the second sealing ring, the base-body surface and the substrate; and

f) introducing an electrolyte through the first opening into the cavity, an electrical connection being formed between the conductive layer and the contact wire.

The method according to the invention forms electrical contact with the back surface of a semiconductor wafer. The electrical contact is in this case formed in the cavity, which runs in the form of a ring on the substrate back surface. It is advantageous in this case that the wet - chemical treatment is limited to the region of the cavity, with the result that the complex handling of the semiconductor wafer in the event of treatment of the entire area of the back surface can be avoided. The conductive layer results in the current which is introduced into the substrate back surface being distributed uniformly over the substrate back surface, allowing a homogeneous flow of current from the substrate back surface to the substrate front surface.

A method step provides for an insulating layer to be disposed on the conductive layer and for an etching substance, which removes the insulating layer from the conductive layer, to be introduced into the cavity. The etching-clear of the conductive layer preferably takes place in the cavity, with

the result that the conductive layer is uncovered in order to make electrical contact.

A further method step provides for a barrier layer to be formed between the substrate and the conductive layer. The barrier layer is used, for example, to prevent the substrate from being contaminated by materials that are disposed in the conductive layer. For this purpose, the barrier layer may, for example, have a diffusion barrier action. Furthermore, it can advantageously be used as a bonding agent for the conductive layer. Furthermore, there is provision for the barrier layer to be conductive.

A further method step provides for the insulating layer to be formed of silicon nitride or silicon oxide and to be etched using an etchant that contains hydrofluoric acid or nitric acid, with the result that the conductive layer is uncovered.

A further method step provides for the insulating layer to be removed by a dry, etching process that uses an etching mask that has been applied to the substrate.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in a configuration and a method for making contact with the back surface of a semiconductor substrate, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

Brief Description of the Drawings:

Fig. 1 is diagrammatic, plan view of a base body with sealing rings and which is suitable for receiving a semiconductor substrate according to the invention;

Fig. 2 is a sectional view taken along the line II-II through the base body illustrated in Fig. 1;

Fig. 3 is a sectional view taken along the line III-III through the base body illustrated in Fig. 1; and

Fig. 4 is a sectional view of a substrate with a conductive layer that has been applied to the substrate back surface.

Description of the Preferred Embodiments:

Referring now to the figures of the drawing in detail and first, particularly, to Fig. 1 thereof, there is shown a base body 21 which has a base-body surface 22. A first sealing ring 23 and a second sealing ring 24 are disposed on the base-body surface 22. The first sealing ring 23 is smaller than the second sealing ring 24, and the first sealing ring 23 is disposed completely inside that region 30 of the base-body surface 22 which is surrounded by the second sealing ring 24. Furthermore, a first opening 26 and a second opening 27 are disposed between the first sealing ring 23 and the second sealing ring 24. The first opening 26 is connected, for example, to an inlet 35, through which gases and liquids can be introduced into the region between the first sealing ring 23 and the second sealing ring 24. The second opening 27 is connected, for example, to an outlet 36, through which liquid and gases can be removed from the space between the first sealing ring 23 and the second sealing ring 24. If, by way of example, a semiconductor substrate 1 is placed onto the first sealing ring 23 and the second sealing ring 24, a cavity 25 is formed, which is delimited by the first sealing ring 23, the second sealing ring 24, the base-body surface 22 and the semiconductor substrate 1. By way of example, gases and

liquids can be introduced into and discharged from the cavity 25 through the first opening 26 and the second opening 27. Fig. 1 also illustrates a third sealing ring 31, which is larger than the first sealing ring 23 and the second sealing ring 24.

Fig. 2 shows a sectional illustration taken along section line II-II. The base body 21 has the base-body surface 22, on which the first sealing ring 23 and the second sealing ring 24 are disposed. The semiconductor substrate 1, which has a first main surface 2 and a second main surface 3, is disposed on the first sealing ring 23 and the second sealing ring 24. The first main surface 2 faces the base body 21 and rests on the first and second sealing rings 23, 24. The first opening 26 and the second opening 27 are disposed in the base body 21, between the first sealing ring 23 and the second sealing ring 24. The first opening 26 is connected to the inlet 35, and the second opening 27 is connected to the outlet 36. The third sealing ring 31 is disposed on the base body 21, and a fourth sealing ring 32 is disposed on the second main surface 3 of the substrate 1. An etching cup 34 is applied to the third sealing ring 31 and the fourth sealing ring 32. A liquid which can wet the second main surface 3 of the substrate 1 and with which electrical contact can be made by a counter electrode 33, can be introduced into the etching cup 34. In the cavity 25 between the first sealing ring 23 and

the second sealing ring 24, a contact wire 28 is disposed on the base-body surface 22 of the base body 21. In addition, there is a bearing 37 on which the substrate 1 can rest when a process liquid is being introduced into the etching cup 34. Fig. 3 presents a sectional illustration taken along the section line III-III shown in Fig. 1. The configuration illustrated in Fig. 3 differs from Fig. 2 in that the first opening 26 and the inlet 35, and also the second opening 27 and the outlet 36, are not disposed on section line III-III.

Fig. 4 illustrates the substrate 1 that has the first main surface 2 and the second main surface 3. By way of example, the first main surface 2 is designated the substrate back surface, and the second main surface 3 is designated the substrate front surface, in which, by way of example, electrical components, such as transistors, capacitors and resistors, are formed. A barrier layer 4 is disposed on the first main surface 2. A conductive layer 5 is disposed on the barrier layer 4. A first insulating layer 6 is disposed on the conductive layer 5, a second insulating layer 7 is disposed on the first insulating layer 6, and a further layer 8 with a surface 9 is disposed on the second insulating layer 7. Further configurations of the configuration illustrated in Fig. 4 are also possible, for example without the barrier layer 4 and without the insulating-layer stack containing the

layers 6, 7 and 8. It is also possible for one or more of the layers 4, 6, 7 and 8 to be provided.

A method for making contact with the back surface of the substrate 1 is described below with reference to Fig. 2. The substrate 1 is placed on top of the first sealing ring 23 and the second sealing ring 24, the surface 9 facing towards the base body 21. The conductive layer 5 is disposed on the first main surface 2 of the substrate 1. If, by way of example, an insulating layer is disposed on the conductive layer 5, an etchant is admitted into the inlet 35 and passes through the opening 26 into the cavity 25, removing the insulating layer 6 from a circular region of the conductive layer 5. In the process, the etchant flows through the cavity 25 to the second opening 27 and through the outlet 36. When the conductive layer 5 has been uncovered in the annular region between the first sealing ring and the second sealing ring, an electrolyte is introduced through the inlet 35 and the first opening 26 into the cavity 25, with the result that electrical contact is formed between the conductive layer 5 and the contact wire 28. Current can then be introduced through the electrolyte into the conductive layer 5 via the contact wire 28, and this current, on account of the good conductivity of the conductive layer 5, can flow, with a uniform distribution over the substrate back surface, uniformly through the substrate 1 to the front surface of the substrate 1. If, by way of example,

a conductive liquid has been introduced into the etching cup 34, the electric current flows onward from the second main surface 3 through the conductive liquid to the counter electrode 33.

After the conductive layer has been etched clear in the annular cavity 25, the cavity 25 can be cleaned and purged, for example with deionized water, before the electrolyte is introduced. After the electrochemical processing of the second main surface 3 has finished, the electrolyte can be removed from the cavity 25, a subsequent purge with deionized water can be carried out, and then drying with nitrogen can take place.

The conductive layer 5 may be formed, for example, from metals or silicides. A suitable metal is, for example, tungsten, while a suitable silicide is, for example, tungsten silicide. It is also possible for the conductive layer 5 to be formed from tungsten nitride. The barrier layer 4 may, for example, likewise be formed from tungsten silicide.